

## Integrated Systems Managing Noise and Spurious within Complex Microwave Assemblies

Application Article written by:  
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During the past 50 years, the microwave industry has grown from infant origins to a multi-billion dollar industry. Our field of study began with a few wizards who discovered the nature of electromagnetic fields and waves. Pioneers used the discovered principles to create wild new machines that allowed communication spanning the globe and detection of incoming hostile aircraft over unthinkable distances. It is still amazing what was accomplished in the early 1950's and 1960's, and we stand in awe at those that laid the foundations for modern microwave engineering disciplines. Those early adventurers began with little more than a slide rule, a keen understanding of the first principles, and a vision to develop solid tools and methods of sound design.

While much of the rigorous analysis techniques necessary to simulate circuits and structures were laid in the late 60's and 70's, the working engineer relied on a fairly limited set of tools, and had only limited, or no access to computers, for simulation. Much of the design work done by the practicing engineer was done using simplified models, extensive prototyping and laboratory experimentation. The lack of computing power available inspired creative normalization methods with graphical renditions. These became known as nomographs (normalized graph). While writing this, I noticed that the word "nomograph" never made it to the electronic dictionary. Most of us, of my "vintage", still have a drawer with a package of paper Smith Charts buried under a stack of cardboard sliding "calculators" yellowed from the last of the smoke filled laboratories. Those sliding cardboard wonders were successful marketing tools of the day, and offered instant pencil free execution of many of the popular nomograph tools that were in common publication and used by working engineers on the bench. Even as I was beginning my career in 1985 (just a young pup in this field), the modern PC was just coming of age. This new tool provided the working RF and Microwave engineer with powerful desktop and bench-top computational tools, allowing automation of the rigorous legacy analysis techniques developed over the previous decades. Most RF engineers recognized the value of the new desktop PC's and took to writing various little routines to improve working efficiency. These often took the form of crude user UN-friendly programs written for HP Calculators, in HP Basic, DOS Quick Basic, Apple Basic or a bootlegged copy of Fortran. I still remember the fun I had with my Commodore 64 and my first copy of RF Circuit Buster (linear s-parameter simulator) from Randy Rhea (Now – Eagleware). With the desktop PC, engineers got their hands on spreadsheet programs such as VisiCalc and Lotus123. As soon as we found that there were extensive math libraries and rudimentary logarithmic plotting capabilities in the spreadsheets, the engagement moved quickly to a shotgun marriage. Modern spreadsheets like Excel and Quattro-Pro have extensive math libraries and graphing capabilities that provide the modern engineer with a quick flexible tool for executing specialized calculations.

Today, we enjoy a profession valued by our nation for microwave guidance technology; secure radio technology, mobile communication and the associated economic growth that the RF and microwave industry has produced. The simulation tools that we

enjoy allow us to predict performance and trade alternative characteristics of various systems before going to the laboratory. The quality of the tools now available from various RF simulation companies in the area of Linear and Non-Linear circuit simulation, Electromagnetic Solvers, and System Simulators is quite amazing. These tools have allowed engineers to produce high yielding complex RF systems and MMIC circuits through 20 GHz and moderate yields through the mmWave bands. However, virtually all complex RF systems with critical carrier noise requirements fail to meet their detailed requirements on the first pass design. Often, this results in many hours in the laboratory, troubleshooting noise and spurious problems. The solutions usually come from understanding the leakage paths from various sources that are causing undesirable characteristics, whether phase noise, spurious, gated phase noise, sensitivity problems, jitter, BER, or symbol error. Resolution of these issues takes its toll on customer satisfaction, management confidence, and reaching the target market in time. There are great synthesis tools available to build a phase locked loop (PLL) model that include the primary noise contribution from the VCO, reference oscillator, divider/phase detector, loop Integrators, resistors. There are no known soft tools that put all of the contributors to noise and spurious together in a single tool. The missing elements tend to be accurate treatment of frequency multiplier chains, the effects of frequency conversion on phase noise performance, DC power supply noise and spurious coupling paths, packaging isolation and PCB layout coupling paths.

I remember a particular design review, where the program manager insisted on certification from our design team that “all” the noise and spurious problems have been resolved on the new board design. It is difficult for those outside our field to understand that, analog RF board designs requiring spurious performance below 70 dB (seven orders of magnitude) and phase noise performance better than  $-140$  dBc/Hz to  $-170$  dBc/Hz (14 to 17 orders of magnitude below the carrier) still have a lot of “best guess” solutions and require iteration to yield producible margins. Engineering ethics and southern upbringing required clarification of his expectations, but it did highlight the gap in our tool set.

RF engineers designing complex converter and frequency synthesizer sub-systems must analyze each noise and spurious contributor separately to gain confidence in proposed designs. Unfortunately, this paper will not provide a unified tool to model all of the gremlins discussed. Our goal is to attempt to systematically address some of the subtle effects that engineers spend so much time chasing. The focus will be on signal generator systems, since those systems usually limit the BER, jitter, or pulsed phase noise performance in communications and Radar systems. In addition, we hope to offer a few useful spreadsheet tools (inherited from our accountant friends), to help predict some of the effects discussed. The technical content is organized to fill in the gaps and provide tools to address each item 1 and 2 in the checklist below. Packaging is beyond the scope of the article.

### Check List for Signal Generator Design Review

#### 1) Requirement Definition

- a) Define all input reference signal source noise and spurious characteristics to the system.
- b) Define all input power supply noise and spurious characteristics to the system.
- c) Define an output phase noise specification in units of dBc/Hz that includes worst case and a goal limit for each local oscillator being generated.
- d) Define an output spurious specification that is consistent with the overall frequency plan of the system in dBc (dB relative to the carrier level)

- e) Define required switching speed and channel size (frequency step) along with a quantifiable verification method.
- 2) Model and Verify**
- a) Model each mixing stage in the conversion for undesirable products using a suitable tool and define filtering needs.
  - b) Model each PLL using a suitable tool and treat it as a block with inputs and outputs defined.
  - c) Model and verify that all multiplier chains and up/down converter phase noise translations support the requirements.
  - d) Model and verify DC power supply inputs have adequate filtering and noise reduction circuitry to meet system phase noise specification and ripple induced spurious requirements.
- 3) Packaging Preparation**
- a) Verify partitioning and shielding is adequate to yield expected performance goals.
    - i) Estimate cavity modes for each isolated compartment and develop mechanical strategies for shifting the modes to frequencies above interest.
    - ii) Estimate coupling mechanisms between separate sections
    - iii) Verify all filtering requirements for spurious products are defined and develop mechanical shielding methods to achieve the rejections required. Model filter cavities for wave guide modes.
  - b) Develop a grounding strategy for executing the PCB layout that includes layering, partitioning within the PCB, minimum via spacing for “hard” ground points, identification of critical groups of components that need to share common grounding nodes.
  - c) Model all critical matching and printed circuit features prior to beginning PCB layout and be prepared to tweak the model as mechanical constraints change.

## SECTION I - REQUIREMENT DEFINITION

It may seem intuitively obvious to define your requirements and goals before a project begins but it almost never happens as cleanly as that. Often system requirements are changing while the RF designs are proceeding. Rather than wait until every thing is defined neatly, engineers are often required to forge ahead in the dawn of a project. What I promote is simple, do your homework, and the homework of others early until you have a set of requirements that are clear enough for you to begin to work in. Spend some time with the systems engineers or customers and get a sense of the range of uncertainty in the critical requirements area. Do some analysis on your own to try to define what you expect is achievable verse what might be required by an application. Develop a cost model and develop a clear picture in your mind about the performance cost drivers. Methodically define each input to your signal generator sub-system and each output as shown in Figure 1 and Table 1.

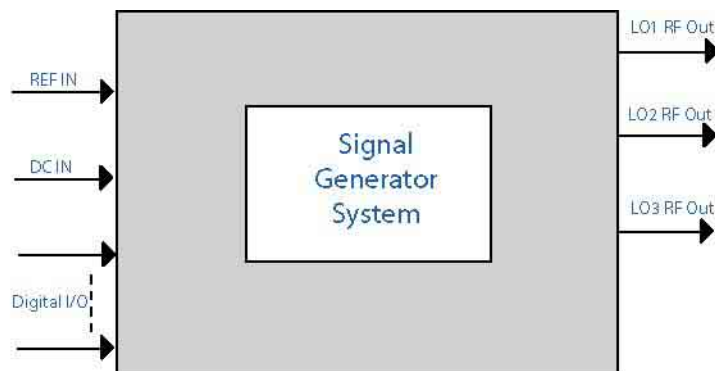


Figure 1: Typical IN/OUT Block Diagram of a Frequency Subsystem

DC Input	RF Ref Input	RF Output	Transfer Characteristic	Logic I/O
<b>Voltage limits</b> Nom/Min/Max % variation Turn-on rise time	<b>Power Level</b> Nom/Min/Max X dBm +/- Y dB	<b>Power Level</b> Nom/Min/Max X dBm +/- Y dB	<b>Switching Speed</b> Define control edge to RF condition, for example 50% TTL to 10 degrees phase settled and 1 dB	<b>Define Serial/Par Control Definition with naming convention.</b>
<b>Current Limits</b> Min/Max Max Peak Current	<b>Phase Noise</b> dBc/Hz SSB or integrated over BW	<b>Phase Noise</b> dBc/Hz SSB or integrated over BW	<b>Pulsed</b> On/Off Ratio Rise/Fall times Delay Time	<b>Define Logic Family</b>
<b>Ripple Input</b> Switching Freq. Peak ripple Ripple freq. Range Periodic spikes	<b>Spurious Input</b> Identify any leakage products from other assemblies that may be present. Quantify in dBc at specific offset	<b>Spurious Output</b> Identify a complete mask to be presented to next assembly. Quantify in dBc at specific offset	<b>Other Unique Modulation</b>	<b>Timing and Control state definition</b>
<b>Input Noise</b> 1) Max total noise over BW  2) Noise power at each offset frequency from the supply	<b>Frequency Stability</b> Drift Vs temperature Drift Vs Life Short term Allen var. Fo +/- X ppm	<b>Frequency Stability</b> Drift Vs temperature Drift Vs Life Short term Allen var. Fo +/- X ppm		<b>Determine if differential control is required to achieve timing accuracy</b>
	<b>Source Impedance</b> Source VSWR Expected Load Frequency Pulling	<b>Source Impedance</b> Source VSWR Expected Load Frequency Pulling		

Table 1. Typical IN/OUT Requirements for a Frequency Subsystem

The requirements that we want to look closely at in this article are the phase noise contributors and spurious along with the defined noise on the DC supply including its ripple characteristics.

## SECTION II – MODEL and VERIFY THE ARCHITECTURE

In new frequency sub-systems, the critical characteristics to model include; realizability of the frequency plan, Mixing product modeling, PLL phase noise and settling time modeling, Multiplier chain phase noise modeling, and DC power supply noise modeling.

Architecture origination is a complex subject that exceeds the scope of the article. Our goal here is to develop the tools to evaluate any given solution. In brief, architecture origination includes; trading several general solutions for the primary noise and switching speed requirements, blocking out the architecture, trading multiple technologies for each block, and confirming realizability. Realizability of a frequency plan solution must be validated for performance margin, parts availability, manufacturability and cost metrics.

## Mixing Product Modeling

Precision signal generators normally have a frequency plan that includes frequency conversion by mixing and multiplication. Modeling of mixing products can be done using various tools, but all are subject to validation of the selected mixer characteristics, at the specific operating levels. It is useful to start your analysis with a known mixer model, with product levels defined for the  $N \times RF \pm M \times LO$  through at least 7<sup>th</sup> or 8<sup>th</sup> order products. An excellent soft tool for this is SPURPLOT (Artech House, Robert R. Kyle) which allows double conversions and user defined mixer tables. Also SPURPLOT has a nice filter definition function built in to help you develop individual specifications for your filters. As the design solidifies it is preferred to get measured mixer data for use in the application. Figures 2 and 3 are examples of the typical output available.

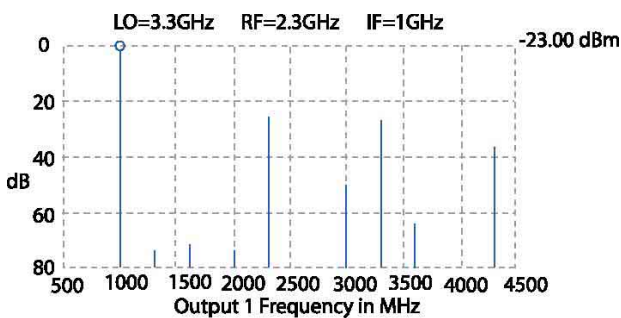


Figure 2: Typical Mixer Spurious Plot

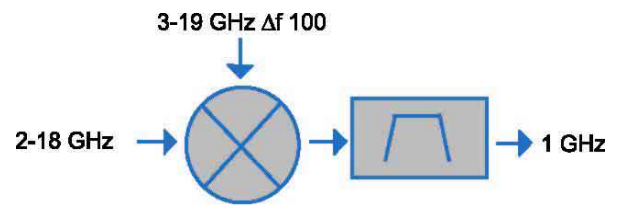


Figure 3: Block Diagram of Figure 2

In either a down conversion or an upconversion the mixer should be treated as a phase noise summation node of the two input ports of the mixer being used. It should also be given a residual noise contribution equivalent to its effective noise figure (conversion loss) and flicker noise ( $1/f$  noise) contribution. These effects can be ignored when the signal levels are high at both ports of the mixer, but make sure in your analysis that it genuinely is not important. Sometimes in an effort to reduce a certain spurious product the drive levels to a mixer can be adjusted to remove the spurious problem, but this can cause problems when the conversion S/N levels get within 10-15dB of the noise floor of the conversion stage. It is straight forward to determine additive equivalent net noise from two sources ( $PN_{total} = PN_A + PN_B$ ). This must be done in absolute power units such as watts or milliwatts to add the powers then reconverted to dBm as follows;  $[PN_{total\ dBc} = P_{carrier\ dBm} - PN_{total\ dBm}, PN_{total\ dBm} = 10 \cdot \text{Log} (10^{((PN_A\ dBm)/10)} + 10^{((PN_B\ dBm)/10)})]$ . The general expression for the additive contribution of noise source A, X dB below noise source B can be derived from simple sum of powers. The resulting expression is as follows:

$$F_{dB} = 10 \cdot \text{Log} \left( 1 + 10^{(-X/10)} \right) \text{ and as shown in Figure 4.}$$

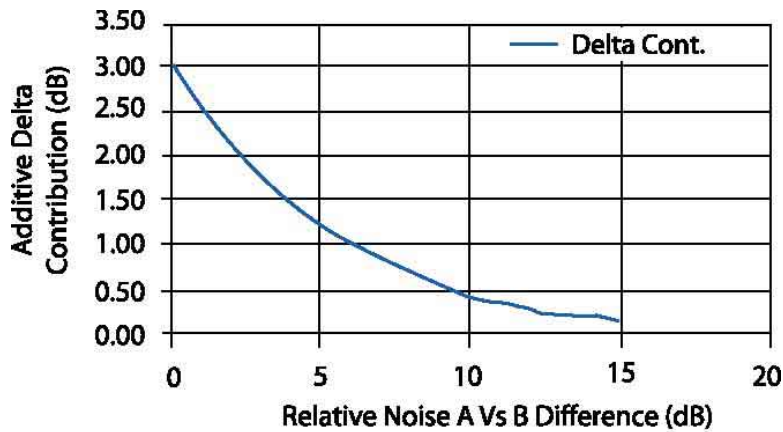


Figure 4: Noise Contribution From Two Sources

X= the noise difference between two sources in dB

This is a helpful chart to paste on the wall in the lab near the phase noise test gear to account for test source noise contribution.

### PLL Modeling

Modeling of PLL sub-circuits has been exhaustively covered by numerous authors because of its importance as an RF building block. We will treat it as a block in our discussion for simplicity. The circuit design techniques involved cross several technical fields including digital sampling, analog operational amplifiers, control systems and oscillator design/ characterization. The PLL simulator tool provided by Randy Rhea (Eagleware ) is cost effective and accurately includes most key noise contributors such as resistor noise, Integrator noise, VCO Noise, Reference noise, divider and PD noise. An example of a simple 2000MHz PLL is shown in Figure 5 with 10kHz closed loop band width. Phase noise verses offset data from a PLL simulation can be extracted and used as a block in the overall signal generator noise analysis as will be shown later.

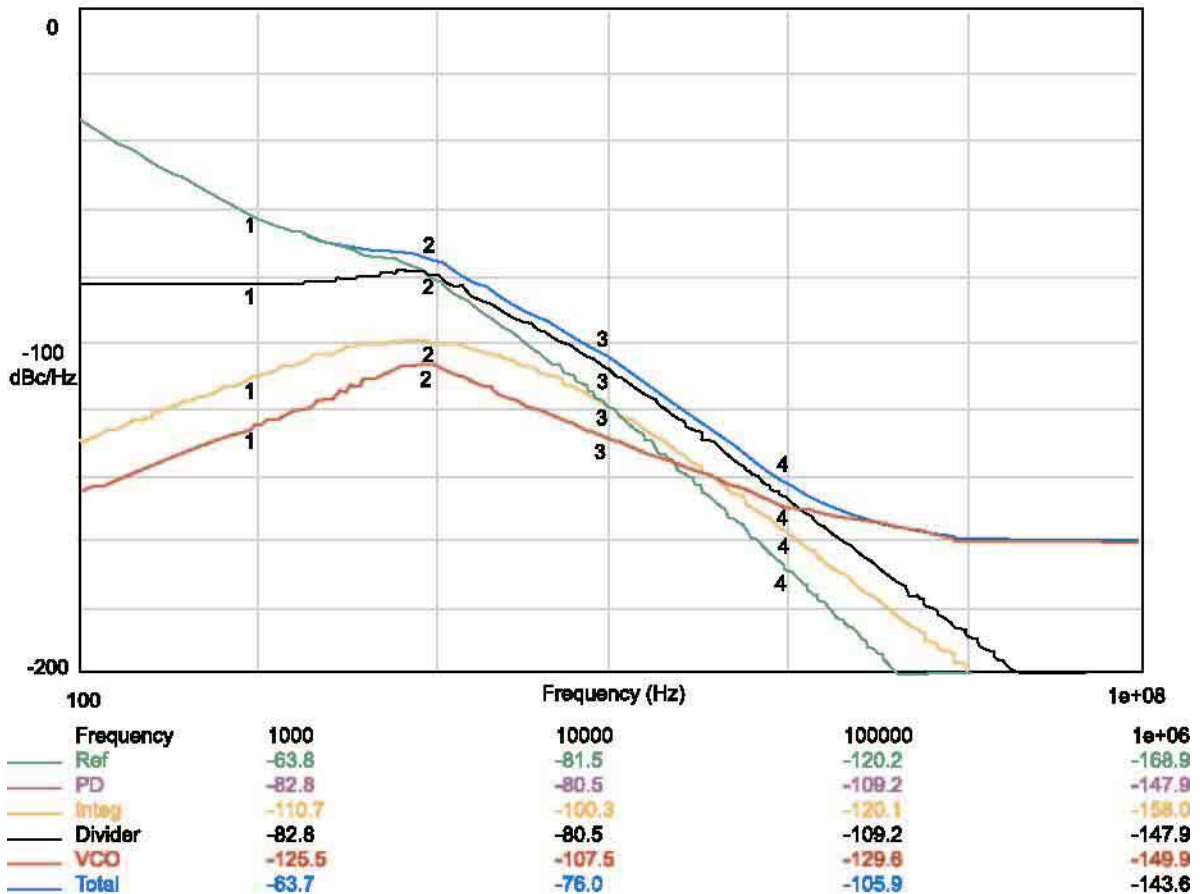


Figure 5: Example PLL Simulation

### Multiplier Modeling

Frequency multipliers are fundamental building blocks of most microwave high performance systems. As components, they come in the form of Step Recovery Diode (SRD) multipliers, Schottky diode varistor multiplier, BJT transistor multipliers, FET Multipliers, YIG Multipliers and Varactor Multipliers. All multipliers use the non-linear characteristics of the particular technology selected to create harmonically rich spectrum. The desired products can be selected from the spectrum and undesired products must be rejected. A common physical property of all multipliers, regardless of technology, is the characteristic translation of delta phase changes from the input to output. The translation of phase is linear with multiplication factor ( $d\phi_{out} = N * d\phi_{in}$ ). Multipliers are not capable of warping time, so doubling or tripling the phase change per unit time translates to doubling or tripling the frequency since frequency is just the term we use for rate of phase change ( $F = d\phi/d\tau$ ). This seems intuitive but the consequences of this simple fact are ignored in the design phase too often, except for the desired effect of frequency multiplication. The undesired effects come in the form of ignored modulation terms and spurious translation.

## Multiplier Phase Noise Modeling

Given that phase noise can be described as a statistically determined spectral phase modulation mask superimposed on an ideal carrier. The instantaneous phase fluctuations are multiplied by  $N$  which in the noise power domain is a  $20 \cdot \log(N)$  function. This means that the input noise of a multiplier block is translated to the output by summing all noise sources present at the effective input, then increasing this noise power by  $20 \cdot \log(N)$ . The noise sources to consider for summation before adding the  $20 \log(N)$  factor include, input phase noise,  $kTB + NF$  Noise, and device  $1/f$  noise from amplifier or multiplier stages. The summation must be done with all terms converted to a common unit of absolute power. The simplified signal flow diagram shown in Figure 6 is the basis for the Excel spreadsheet tool available by request from TRAK Microwave Corp [www.trak.com](http://www.trak.com).

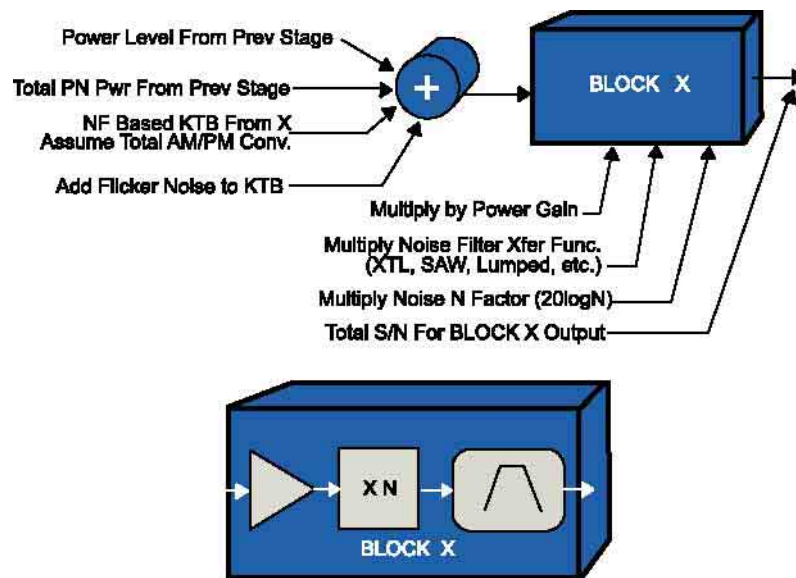
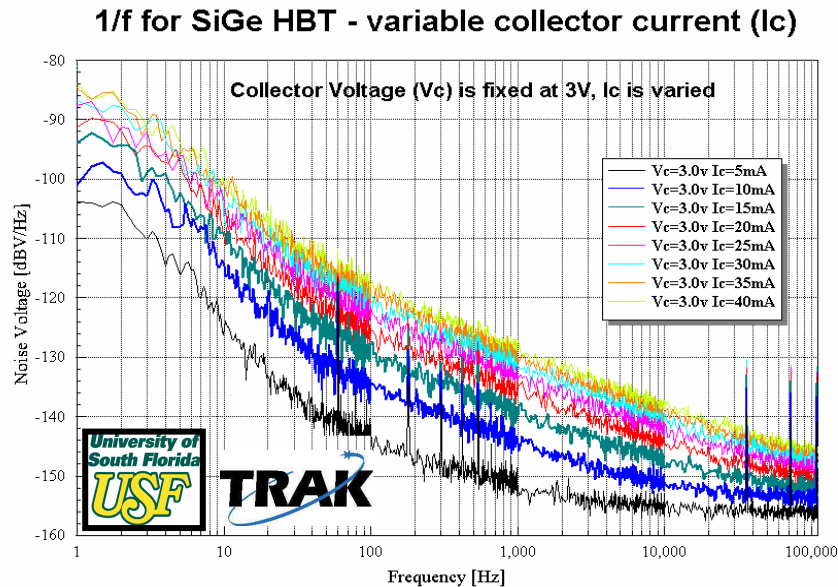


Figure 6: Simplified Multiplier Signal Flow Diagram





### Multiplier Spurious Modeling

Similarly, multipliers take the instantaneous phase deviation associated with spurious products injected at the input or interstage from bias ripple, then multiply the deviation by N to the output. This means that a signal source, such as a crystal oscillator at 80MHz, feeding the input to a X128 multiplier to X-Band would need to have PM/FM spurious products lower than -102 dBc to achieve an X-Band spectrum that has all spurious less than -60 dBc (given  $20 \cdot \log(128) = 42$  dB). This is caused by the direct multiplication by N of the angular deviation of peak phase deviation. Another subtle effect of a similar nature occurs when amplifiers or active multiplier stages are modulated by DC bias ripple or noise which we will address in the next section.

### DC Power Supply Noise and Spurious Coupling

DC power supplies can severely hurt the performance of precision RF sources if not managed carefully. It is critical to understand both ripple and noise to design adequate attenuation to prevent modulating the RF sub-blocks within the system. First we will review some foundational concepts of noise voltage, then we will be able to address the coupling of noise voltage to phase noise and spurious effects.

All electronic devices produce a noise power. The one we are all most familiar with is the noise power at room temperature:

$$N_t = kTB$$

$N_t$  is noise power in watts

Boltzmann's Constant  
Temperature  
Band Width

$k = 1.38 \times 10^{-23}$  W-s/K,  
 $T =$  room temp  $17^\circ\text{C} + 273^\circ\text{C} = 290\text{k}$   
 $B =$  Noise bandwidth for normalization (1 Hz)

$$N_t = 4 \times 10^{-21} \text{ W in 1 Hz BW}$$

Converting to mW  $N_t = (4 \times 10^{-21} \text{ W}) * (1000 \text{ mW/W}) = 4 \times 10^{-18} \text{ mW}$  in 1 Hz BW

Converting to dBm  $N_t = 10 * \text{Log} (4 \times 10^{-18} \text{ mW}) = -174 \text{ dBm/Hz}$

This is the basis for cascaded noise calculations in receivers and local oscillator multiplication chains. The noise figure of a device is simply the characteristic effective input noise power ratio, relative to  $-174 \text{ dBm/Hz}$ . This is a good number to commit to memory since it can be easily scaled to other measurement bandwidths. Many analyses tools in use today handle cascaded receiver noise very well. The subject is brought up here just to remind us of the basic physics built into the universe we work in and to provide some background to cascaded multiplier network discussion and other phase noise contributors. It is often helpful to convert thermal noise within a resistor into a noise voltage for circuit and system analysis.

The simplified expression for resistor noise voltage is as follows:

$$V_t = \sqrt{4kTRB}$$

$V_t$  = rms noise voltage

$k = 1.38 \times 10^{-23} \text{ W-s/K}$ , Boltzmann's Constant

R = selected resistance in ohms

T = room temp  $17\text{C} + 273\text{C} = 290\text{k}$

B = normalized noise bandwidth in Hz

Calculate for a 1000 ohm resistor

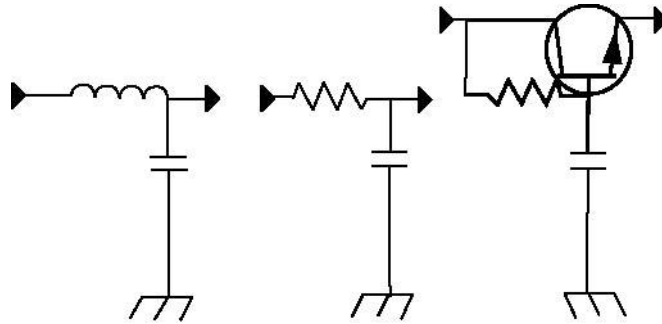
$$V_t = \text{SQRT} (4 * 1.38 \times 10^{-23} * 290 * 1000 * 1) = 4 \text{ nV}/\sqrt{\text{Hz}}$$

This result is useful to memorize also, since it can scale by the square root of the resistance ratio and to other bandwidths. When using resistors in bias networks or RC filter networks keep this in mind because large value resistors are noise generators. Operational amplifier input noise is usually specified in these terms. For example, the classic OP-27 is specified to have about  $3.5 \text{ nV}/\sqrt{\text{Hz}}$ , which can be translated by circuit gain. Voltage regulator circuits are usually specified in terms of total noise ( $\sim 10 \text{ uVrms}$ ) within their bandwidth so to estimate the equivalent noise in a 1 Hz BW simply divide by square root of the regulator output bandwidth.

$$V_{\text{reg noise}} = 10 \text{ uVrms} / \sqrt{(10 \text{ kHz})} = 100 \text{ nV}/\sqrt{\text{Hz}}$$

It is not uncommon to find families of regulators that have  $200\text{-}300 \text{ nV}/\sqrt{\text{Hz}}$ . This is due to the scaling nature of linear regulator designs from an internal noise reference voltage. Noise voltage in systems must be managed tightly to achieve difficult phase noise requirements normally expected in modern systems. Active or passive RC filters can be used to attenuate noise to meet the system requirements.

Typical Noise Clean up circuits are shown in Figure 9.



**Figure 9: Noise Clean Up Circuit Examples**

To use the voltage noise concepts we need a transfer function from noise voltage to AM/FM/PM noise. This article will focus on the dominate mechanisms so we will ignore AM contributions since they are almost always less significant and get converted to FM/PM noise through imperfect non-linear limiting devices. Frequency and phase modulated signals can be expressed by a Bessel function and for small angle modulation  $\beta \ll 1$  the linear approximation can be shown to be reasonably accurate for spurious and noise power products less than  $-30\text{dBc}$ . Shown below is the linear approximation to the Bessel functions.

FM Modulation: ( $dF$  = peak frequency deviation,  $F_m$  = modulation rate or ripple frequency)  
 $SpuriousSSB_{dBc} = 20 \cdot \text{Log}(dF / (2 \cdot F_m))$

PM Modulation: ( $d\theta$  = peak phase deviation )  
 $SpuriousSSB_{dBc} = 20 \cdot \text{Log}(d\phi / 2)$

From this we can use power supply ripple specification to calculate PM or FM spurious. Use FM spurious calculations for oscillator blocks that have frequency/volt deviation sensitivities such as VCO or crystal oscillator pushing and tuning sensitivities.

Example 1: Crystal oscillator at 80MHz with a tuning sensitivity of 10ppm/volt and pushing of 1ppm/volt. Given a switching DC power supply with 100mV pk ripple at 100kHz rate used as the tune voltage. Find SSB spurious.

$$\text{Use FM equation: } SSB = 20 \cdot \text{Log}((100e-3 \cdot 10e-6 \cdot 80e6) / (2 \cdot 100e3)) = -68 \text{ dBc}$$

Example 2: Amplifier made from MESFET microwave transistor has a sensitivity of 10deg/volt of bias change. Given the same DC converter described in example 1. Find the SSB spurious.

$$\text{Use PM equation: } SSB = 20 \cdot \text{log}(((100e-3 \cdot 10 \cdot \pi / 180) / 2)) = -41 \text{ dBc}$$

Phase Noise can be similarly calculated from noise voltage generated by DC power supplies when coupled to oscillator circuits by using the FM equation above modified to convert the rms noise voltage to peak voltage.

### Phase Noise In Oscillators from Noise Voltage:

( $K_v$ = tuning sensitivity Hz/volt,  $V_n$ =noise voltage nV/ $\sqrt{\text{Hz}}$ ,  $F_m$ = offset frequency from carrier and frequency associated with  $V_n$ .)

$$\text{PhaseNoiseSSB}_{\text{dBc/Hz}} = 20 \cdot \text{Log} \left[ \frac{K_v \cdot \sqrt{2} \cdot V_n \cdot 1e-9}{2 \cdot F_m} \right]$$

#### Example 3:

VCO at 800MHz with a pushing sensitivity of 100kHz/volt. Given a switching DC power supply, with 126.5nV/ $\sqrt{\text{Hz}}$  noise at 25kHz offset used as the tune voltage. Find phase noise 25kHz from the carrier due to power supply noise.

Use Phase Noise equation:

$$\text{SSB dBc/Hz} = 20 \cdot \text{Log}((100e3 \cdot \sqrt{2} \cdot 126.5 \cdot 1e-9)/(2 \cdot 25e3)) = -128 \text{ dBc/Hz}$$

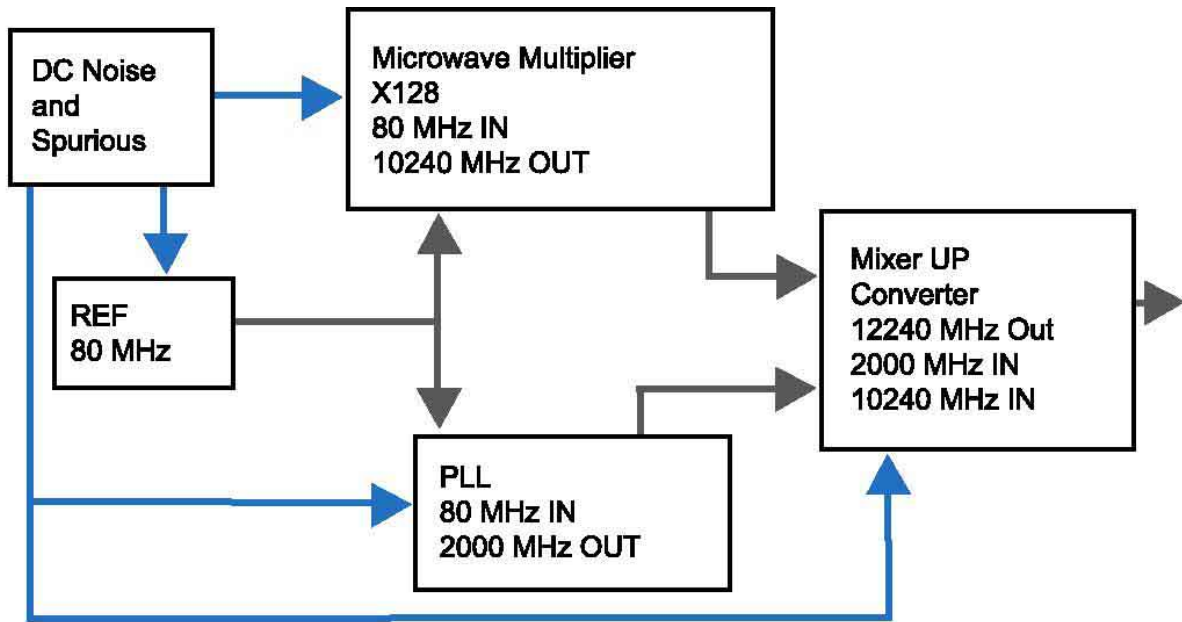
### Noise and Spurious in PLL Blocks

A phase locked loop (PLL) functions as both a multiplier and a tracking filter relative to the reference input. This means all noise and spurious riding on the reference will be multiplied by the effective N ( Effective N =  $N_{\text{VCO}}/N_{\text{ref}}$  ) of the PLL to its output within the control band width and attenuate reference related spurious and noise outside the loop BW by approximately 20dB/decade. This can be used to your advantage if you are supplied a reference source that is too noisy or has spurious far from the carrier.

If the noise is injected into the VCO or post amplifiers within the control loop there is some significant attenuation possible. The loop will not attenuate their effects beyond the control BW, but will attenuate the spurious or noise on the VCO increasing -40dB/decade within  $\frac{1}{2}$  loop BW as you go towards the carrier. This is why a PLL improves the phase noise of a VCO within the BW. This same effect works to attenuate spurious, noise and vibration induced problems superimposed on the VCO. The approximations to the attenuation are easy to implement within a spread sheet, although a more rigorous solution would be to use the calculated loop transfer function.

### Building a Good System Model

This can be very complex, so we will limit our discussion to setting up a model for a basic system. An Excell spread sheet is an excellent way to use the formulas and solutions offered to quickly build a spurious and noise model for a custom application. Start with a high level block diagram and an input phase noise/DC Noise specification. From there you can use the concepts discussed to build a total noise model for the converter system local oscillator. A simple model as shown in Figure 10 will help organize your spread sheet math model.



**Figure 10: Simple Noise Model - Used to Build a Spread Sheet Converter System**

### Conclusions

The goal of this article was to provide a methodical way of managing noise and spurious in complex source based subsystems such as converters. The checklist suggested provides a good tool, if used for design review purposes. It is always helpful at the beginning of the design to make sure a clear connection between the expected performance of the microwave assembly and the supplied coherent reference source and the available DC power supplies. Additional tools were offered to calculate cascaded phase noise and formula were suggested to predict power supply noise and spurious effects. The complex subject of package isolation was only briefly mentioned in the suggested checklist but is very important in control of cross talk and spurious coupling within tightly integrated assemblies. Package isolation is a subject that has become more critical and risky as cell-phone handsets shrink and military equipment is designed into SEM-E or VME Euro cards. It is hoped the compilation of commonly known principles offered here, will help microwave subassembly designers, get it done right, and get it done sooner. Then we can all spend more time with our families and less time chasing birdies late at night behind schedule.

William F. Graves: Bio-Sketch

Bill Graduated from University of South Florida with a BSEE degree in 1985, he has been involved in design and management of RF/Microwave low phase noise subassemblies for RADAR systems and Microwave SATCOM for 18 years. He has worked at Lockheed Martin Orlando Missile Systems, Raytheon St. Petersburg and TRAK Microwave. Bill is currently Chief Technology Officer of TRAK Microwave located in Tampa FL.

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